What is Claimed is:

1. A semiconductor device comprising:

a substrate having a chip mounting surface and a package surface;

a semiconductor chip mounted on the chip mounting surface;

wherein the semiconductor chip includes;

a plurality of electrode pads formed on a circuit forming surface of the semiconductor chip,

an insulating layer which is formed on the circuit forming surface and which includes an opening for exposing a part of the surface of each electrode pad,

a plurality of conductive posts disposed over the insulating layer, and

re-distribution wirings formed on the insulating layer to electrically connect the conductive posts to the electrode pads,

external terminals disposed on the package surface;

substrate pads formed on the chip mounting surface so as to correspond the conductive posts;

internal wirings formed on the chip mounting surface to electrically connect the substrate pads and the external terminals; and

a sealing resin for sealing the chip mounting surface and the semiconductor chip.

2. The semiconductor device according to Claim 1, wherein the interval between the conductive posts is wider than that between electrode pads, and the interval between the external terminals is wider than that between the conductive posts.

3. The semiconductor device according to Claim 1, wherein a back surface of the semiconductor chip is exposed.

4. The semiconductor device according to Claim 1, wherein the external terminals comprise solder balls.

5. A semiconductor device

a substrate having a chip mounting surface and a package surface;

a first semiconductor chip mounted on the chip mounting surface;

wherein the first semiconductor chip includes;

a plurality of first electrode pads formed on a first circuit forming surface of the first semiconductor chip,

an insulating layer which is formed on the first circuit forming surface and which includes an opening for exposing a part of the surface of each first electrode pad,

a plurality of conductive posts disposed over the insulating layer, and

re-distribution wirings formed on the insulating layer to electrically connect the conductive posts to the first electrode pads,

a second semiconductor chip mounted on a back surface of the first semiconductor chip and having a plurality of second electrode pads formed on a second circuit forming surface of the second semiconductor chip;

external terminals provided on the package surface;

substrate pads formed on the chip mounting surface so as to correspond the conductive posts;

bonding posts formed on the chip mounting surface;

bonding wires for connecting the second electrode pads to the bonding posts;

internal wirings formed on the chip mounting surface for electrically connecting the substrate pads and the bonding posts to the external terminals; and

a sealing resin for sealing the chip mounting surface, the bonding wires, and the first and second semiconductor chips.

6. The semiconductor device according to Claim 5, wherein the interval between the conductive posts is wider than that between first electrode pads, and the interval between the external terminals is wider than that between the conductive posts.

7. The semiconductor device according to Claim 5, wherein the external terminals comprise solder balls.

8. A semiconductor device comprising:

a substrate having a first surface and a second surface opposed to the first surface;

a semiconductor chip having a third surface and a fourth surface opposed to the third surface, and mounted on the first surface;

wherein the semiconductor chip includes;

a plurality of electrode pads formed on the third surface,

an insulating layer which is formed on the third surface and which includes an opening for exposing a part of the surface of each electrode pad,

a plurality of bump electrodes disposed over the insulating layer, and

wirings formed on the insulating layer to electrically connect the bump electrodes to the electrode pads,

external terminals disposed on the second surface;

substrate pads formed on the first surface;

conductive traces formed on the first surface to electrically connect the substrate pads and the external terminals; and

a sealing resin for sealing the first surface and the semiconductor chip.

9. The semiconductor device according to Claim 8, wherein the interval between the bump electrodes is wider than that between electrode pads, and the interval between the external terminals is wider than that between the bump electrodes.

10. The semiconductor device according to Claim 8, wherein the fourth surface of the semiconductor chip is exposed.

11. The semiconductor device according to Claim 8, wherein the external terminals comprise solder balls.

12. A semiconductor device

a substrate having a first surface and a second surface opposed to the first surface;

a first semiconductor chip having a third surface and a fourth surface opposed to the third surface, and mounted on the first surface;

wherein the first semiconductor chip includes;

a plurality of first electrode pads formed on the third surface,

an insulating layer which is formed on the third surface and which includes an opening for exposing a part of the surface of each first electrode pad,

a plurality of bump electrodes disposed over the insulating layer, and

wirings formed on the insulating layer to electrically connect the bump electrodes to the first electrode pads,

a second semiconductor chip having a fifth surface and a sixth surface opposed to the fifth surface and having a plurality of second electrode pads formed on the fifth surface, the sixth surface being mounted on the fourth surface;

external terminals provided on the second surface;

substrate pads formed on the first surface;

bonding pads formed on the first surface;

bonding wires for connecting the second electrode pads to the bonding terminals;

conductive traces formed on the first surface for electrically connecting the substrate pads and the bonding pads to the external terminals; and

a sealing resin for sealing the first surface, the bonding wires, and the first and second semiconductor chips.

13. The semiconductor device according to Claim 12, wherein the interval between the bump electrodes is wider than that between first electrode pads, and the interval between the external terminals is wider than that between the bump electrodes.

14. The semiconductor device according to Claim 12, wherein the external terminals comprise solder balls.